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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,525	06/02/2000	Ying-Chou Tsai	JCLA5827	6171

7590 04/13/2004

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,525	TSAI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 5, 7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lan et al. (6,034,427).

Lan et al. teach in figure 2B and related text a substrate structure of flip chip package comprising a plurality of patterned circuit layers 217 connected by vias 221A-M in an insulative layer, at least an insulative layer 221 stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of first mounting pads 223A, 223B and plurality of a second mounting pads 224A (figure 2F) and

a solder mask layer 229 covering the patterned circuit layer on the surface of the substrate of the package, the solder mask layer partially covering a first top surface of the first mounting pads 223A, 223B by being in direct contact with entire sidewalls and a portion of the top surface of the first mounting pads while entirely exposing a second top surface and sidewalls of the second mounting pads 224A and the whole surface of the second mounting pad, wherein the first mounting pads 223A, 223B are disposed at a

periphery region of the substrate (figure 2F) and the second mounting pads 224A are disposed at a central region of the substrate, and the first mounting pads surround all of the second mounting pads, and wherein said first and second mounting pads are for electrically contacting with corresponding bumps of a chip.

Lan et al. do not state in the embodiment of figure 2 that the device is used in a flip chip package.

Lan et al. teach that it known to use a flip chip structure in a BGA packages. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Lan et al.'s device in a flip chip structure, in order to use the device in an application, which requires a flip chip structure.

Regarding the claimed limitations of using the first and second mounting pads for electrically contacting corresponding bumps of a chip, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 5, 7 and 13, the device of Lan et al. comprises a chip 213 having an active surface with a plurality of bumps 211 disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second

bonding pads respectively and an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package, wherein the bumps attach only to the top surface of the first mounting pads.

2. Claims 2-4, 8-10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lan et al. in view of Admitted Prior Art (APA).

Lan et al. and teach substantially the entire claimed structure, as applied to claims 1 and 7 above, except bumps attach to both the top surface and side surfaces of the second mounting pads.

APA teaches in figure 2 a BT substrate structure of flip chip package wherein each of the patterned circuit layer is formed by a copper foil layer defined by photo lithographic and etching processes, and bumps attach to both the top surface and side surfaces of the second mounting pads (pages 1-2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to attach bumps to both the top surface and side surfaces of the second mounting pads in Lan et al.'s device in order to increase the contact area between the bumps and the second mounting pads.

Regarding claims 4 and 10, APA teaches that the pitch of the first mounting pads is smaller than the pitch of the second mounting pad (pages 2-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the pitch of the first mounting pads smaller than the pitch of the second mounting pad in

Lan et al.'s device in order to reduce short circuits in the device by preventing the formation of bridges across adjacent pads.

3. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lan et al. in view of Katchmar (6,194,782).

Lan et al. teach substantially the entire claimed structure, as applied to claims 1 and 7 above, except the pitch of the first mounting pads being smaller than the pitch of the second mounting pad.

Katchmar teaches in figure 5 the pitch of the first mounting pads (of bumps 40) is smaller than the pitch of the second mounting pad (of bumps 24). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the pitch of the first mounting pads smaller than the pitch of the second mounting pad in Lan et al.'s device in order to reduce short circuits in the device by preventing the formation of bridges across adjacent pads.

Response to Arguments

4. Applicant argues that bonding pads 224A can not be arranged in central area of the package substrate because the chip is mounted in the central area and the chip is electrically connected with the package substrate via the bonding wires 227A.

Figure 2F clearly depicts bonding pads 224A are arranged in a central area of the package substrate, with respect to the first mounting pads which surround the second mounting pads.

5. Applicant argues that the second mounting pads are not used for electrically contacting with corresponding bumps of a chip, because Lan et al. teach that bonding pads 224A are for attaching the bonding wires 227A.

Although Lan et al. teach that bonding pads 224A are for attaching the bonding wires 227A, the various bonding pads in the electrical circuit of a package are all electrically interconnected to external sources, and thus the first and second mounting pads are electrically contacting with corresponding bumps of a chip.

Note that the broad recitation of the claim does not require the mounting pads to direct contact with corresponding bumps of a chip.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
April 8, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800